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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/826,240	04/04/2001	Anil Kavipurapu	KAVIPURAPU 1	4102

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EXAMINER	
YANCHUS III, PAUL B	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 10/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/826,240	KAVIPURAPU, ANIL	
	Examiner	Art Unit	
	Paul B Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This final office action is in response to amendments filed on 7/7/04.

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 and 8-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Atkinson, US Patent no. 6,233,691.

Regarding claim 1, Atkinson teaches a power selection system for use with a reconfigurable circuit [CPU chip], comprising:

a monitoring circuit [activity monitor logic] configured to monitor an operating characteristic [cache read misses] associated with at least one node located within said reconfigurable circuit; and

a mode selection circuit [power management logic] coupled to said monitoring circuit and configured to select one of:

a normal power mode when said operating characteristic falls within a predetermined operating range of said reconfigurable circuit [cache read hit rate is lower than a certain level], and

an alternative power mode [reduced system clock frequency to reduce power consumption] when said operating characteristic falls outside of said predetermined operating range of said reconfigurable circuit [cache read hit rate rises above a certain level, column 4, lines 35-67 and column 7, lines 25-35], said alternative power mode obtained by adapting said reconfigurable circuit [adjusting the frequency of the clock frequency supplied to the microprocessor portion of the CPU, column 4, lines 24-34].

Atkinson teaches a power selection system for use in a reconfigurable CPU chip. Specifically, Atkinson teaches changing the CPU power mode to a low power mode by adapting clock control circuitry in the CPU to reduce the frequency of the clock signal supplied to the microprocessor portion of the CPU [column 4, lines 24-34].

Regarding claim 2, Atkinson teaches a counter which counts the number of times a CACHE_MISS signal is asserted in a predetermined amount of time [column 5, line 5 – column 6, line 45].

Regarding claim 3, Atkinson teaches a predetermined operating range which falls below a certain threshold value [slow comparison value, column 7, lines 25-35].

Regarding claim 4, Atkinson teaches counting the number of times a CACHE_MISS signal is asserted in a predetermined amount of time. The counted number represents the amount of times a cache read miss occurs. Atkinson teaches setting an alternative power mode when the counted number of cache read misses are below a certain threshold value and remaining in a

normal power mode when the counted number of cache read misses are not below a certain threshold value [column 7, lines 25-35]. However, changing to the alternative power mode when the number of cache read misses are below a certain threshold value is equivalent to changing to the alternative power mode when the number of cache read hits are above that same threshold value. Atkinson also explicitly teaches changing to an alternative power mode [reducing the system clock speed to reduce power consumption] when the cache read hits are above a certain threshold value [column 4, lines 62-67].

Regarding claim 5, Atkinson teaches monitoring cache misses during a preset period of time [column 4, lines 55-62].

Regarding claim 6, Atkinson teaches reducing the system clock speed to reduce power consumption when the cache read hits are above a certain threshold [column 4, lines 62-67].

Regarding claim 8, Atkinson teaches a power selection method for a reconfigurable circuit [CPU chip], comprising:

monitoring [activity monitor logic] an operating characteristic [cache read misses] associated with at least one node located within said reconfigurable circuit; and

selecting one of:

a normal power mode when said operating characteristic falls within a predetermined operating range of said reconfigurable circuit [cache read hit rate is lower than a certain level], and

an alternative power mode [reduced system clock frequency to reduce power consumption] when said operating characteristic falls outside of said predetermined operating range of said reconfigurable circuit [cache read hit rate rises above a certain level, column 4,

lines 35-67 and column 7, lines 25-35], said alternative power mode obtained by adapting said reconfigurable circuit [adjusting the frequency of the clock frequency supplied to the microprocessor portion of the CPU, column 4, lines 24-34].

Atkinson teaches a power selection method for use in a reconfigurable CPU chip. Specifically, Atkinson teaches changing the CPU power mode to a low power mode by adapting clock control circuitry in the CPU to reduce the frequency of the clock signal supplied to the microprocessor portion of the CPU [column 4, lines 24-34].

Regarding claim 9, Atkinson teaches a counter which counts the number of times a CACHE_MISS signal is asserted in a predetermined amount of time [column 5, line 5 – column 6, line 45].

Regarding claim 10, Atkinson teaches a predetermined operating range which falls below a certain threshold value [slow comparison value, column 7, lines 25-35].

Regarding claim 11, Atkinson teaches counting the number of times a CACHE_MISS signal is asserted in a predetermined amount of time. The counted number represents the amount of times a cache read miss occurs. Atkinson teaches setting an alternative power mode when the counted number of cache read misses are below a certain threshold value and remaining in a normal power mode when the counted number of cache read misses are not below a certain threshold value [column 7, lines 25-35]. However, changing to the alternative power mode when the number of cache read misses are below a certain threshold value is equivalent to changing to the alternative power mode when the number of cache read hits are above that same threshold value. Atkinson also explicitly teaches changing to an alternative power mode [reducing the

system clock speed to reduce power consumption] when the cache read hits are above a certain threshold value [column 4, lines 62-67].

Regarding claim 12, Atkinson teaches monitoring cache misses during a preset period of time [column 4, lines 55-62].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson, US Patent no. 6,233,691.

Regarding claims 7 and 13, Atkinson, as described above, teaches a power selection system and method for use with a reconfigurable circuit. Atkinson does not disclose that the reconfigurable circuit comprises a monitored sub-circuit with a delay element and a multiplier, such as a PRBS generator or a digital filter. However, reconfigurable PRBS generators and digital filters are well known in the art. It would have been obvious to one of ordinary skill in the art to apply the power selecting method taught by Atkinson to well known reconfigurable PRBS generators and digital filters in order to reduce their power consumption.

Regarding claims 14, 15 and 20, Atkinson teaches a reconfigurable circuit comprising:

a monitoring circuit [activity monitor logic] configured to monitor an operating characteristic [cache read misses] associated with a sub-circuit located within said reconfigurable circuit; and

a mode selection circuit [power management logic] coupled to said monitoring circuit and configured to select one of:

a normal power mode when said operating characteristic falls within a predetermined operating range of said reconfigurable circuit [cache read hit rate is lower than a certain level], and

an alternative power mode [reduced system clock frequency to reduce power consumption] when said operating characteristic falls outside of said predetermined operating range of said reconfigurable circuit [cache read hit rate rises above a certain level, column 4, lines 35-67 and column 7, lines 25-35], said alternative power mode obtained by adapting said reconfigurable circuit [adjusting the frequency of the clock frequency supplied to the microprocessor portion of the CPU, column 4, lines 24-34].

Atkinson teaches a power selection system for use in a reconfigurable CPU chip. Specifically, Atkinson teaches changing the CPU power mode to a low power mode by adapting clock control circuitry in the CPU to reduce the frequency of the clock signal supplied to the microprocessor portion of the CPU [column 4, lines 24-34].

Atkinson does not disclose that the reconfigurable circuit that comprises a monitored circuit with a delay element and a multiplier, such as a PRBS generator or a digital filter. However, reconfigurable PRBS generators and digital filters are well known in the art. It would have been obvious to one of ordinary skill in the art to apply the power selecting method taught

by Atkinson to well known reconfigurable PRBS generators and digital filters in order to reduce their power consumption.

Regarding claim 16, Atkinson teaches a counter which counts the number of times a CACHE_MISS signal is asserted in a predetermined amount of time [column 5, line 5 – column 6, line 45].

Regarding claim 17, Atkinson teaches a predetermined operating range which falls below a certain threshold value [slow comparison value, column 7, lines 25-35].

Regarding claim 18, Atkinson teaches counting the number of times a CACHE_MISS signal is asserted in a predetermined amount of time. The counted number represents the amount of times a cache read miss occurs. Atkinson teaches setting an alternative power mode when the counted number of cache read misses are below a certain threshold value and remaining in a normal power mode when the counted number of cache read misses are not below a certain threshold value [column 7, lines 25-35]. However, changing to the alternative power mode when the number of cache read misses are below a certain threshold value is equivalent to changing to the alternative power mode when the number of cache read hits are above that same threshold value. Atkinson also explicitly teaches changing to an alternative power mode [reducing the system clock speed to reduce power consumption] when the cache read hits are above a certain threshold value [column 4, lines 62-67].

Regarding claim 19, Atkinson teaches monitoring cache misses during a preset period of time [column 4, lines 55-62].

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER ~~3600~~ 2100

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus
October 7, 2004